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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,370	12/09/1999	LOUIS A. LIPPINCOTT	042390.P7639	8772

8791 7590 03/07/2006

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ART UNIT	**PAPER NUMBER**
2627	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/458,370
Filing Date: December 09, 1999
Appellant(s): LIPPINCOTT, LOUIS A.

Alan Pederson-Giles
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 7, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,268,853	Tanaka	12-1993

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 4-8, 11-15, 19-21, 23-25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (USPN 5,268,853, hereafter Tanaka).

Regarding claim 1, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 13, line 23-25), comprising:

executing first and second one-dimensional inverse discrete cosine transforming functions in first and second separate inverse discrete cosine transforming calculators (4, 6), each of the first and second functions being controlled to operate on a matrix of coefficients (Figure 5; column 5, line 12-33) with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a row direction at a first time (column 11, line 9-15), and with both of said fist and second inverse discrete cosine transforming calculators operating simultaneously in a column direction at a second time (column 11, line 16-40; column 15, line 10-28).

Regarding claim 8, Tanka discloses a storage medium bearing a machine-readable program capable of causing a machine to:

execute two, one-dimensional inverse discrete cosine transforming functions (column 4, line 61-68; column 13, line 23-25) in first and second inverse discrete cosine calculators (4, 6), each of the functions being controlled to operate on a matrix of coefficients (Figure 5; column 5, line 12-33) with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in the row direction at a first time (column 11, line 9-15), and with both of said fist and second inverse discrete cosine transforming calculators operating simultaneously in the column direction at a

second time subsequent to said first time (column 11, line 16-40; column 15, line 10-28).

Regarding claim 15, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 5, line 12-33; column 13, line 23-25), comprising:

first executing a first one-dimensional inverse discrete cosine transforming function on a first inverse discrete cosine calculator (4), in a row direction on a first matrix of coefficients to produce a first matrix of intermediate results (Figure 5; column 11, line 9-15);

second, after said first executing, on said first inverse discrete cosine calculator (4), executing a second one-dimensional inverse discrete cosine transform in a column direction on a second matrix of coefficients to produce another matrix of intermediate results (column 11, line 16-24);

on a second inverse discrete cosine calculator (6), executing a third one-dimensional inverse discrete cosine transforming function in said column direction on the first matrix of intermediate results concurrent with said second executing in the column direction on said second matrix of coefficients (column 11, line 18-40), and

periodically switching and executing between the row and column directions (column 10, line 26-31 and 59-63; column 11, line 16-17; column 15, line 10-28).

Regarding claim 19, Tanaka discloses a storage medium bearing a machine-readable program capable of causing a machine to:

execute a first one-dimensional inverse discrete cosine transforming function (Figure 5, element 4), where the first function executes in a row direction on a first matrix of coefficients, producing a matrix of intermediate results (column 11, line 9-15);

execute a second one-dimensional inverse discrete cosine transform (Figure 5, element 4) in a column direction on a second matrix of coefficients;

execute a third one-dimensional inverse discrete cosine transforming function (Figure 5, element 6), where the second function executes in said column direction on the matrix of intermediate results concurrent with execute a second function on the second matrix of coefficients (column 11, line 18-40),

in which the functions switch periodically and concurrently between the row and column directions (column 10, line 26-31 and 59-63; column 11, line 16-17; column 15, line 10-28).

Regarding claims 23 and 25, Tanaka discloses an apparatus and computer system including a processor implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 5, line 12-33; column 13, line 23-25), comprising:

two (first and second) one-dimensional inverse discrete cosine transform blocks (Figure 5, elements 4 and 6);

a memory block (Figure 5, element 2);

a sequencer block (Figure 6, element 18), the sequencer block alternately being in a first state to control a column direction of operation of both one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation

of both one-dimensional inverse discrete cosine transform blocks (column 10, line 17-31; column 11, line 9-20); and

an address generator block (Figure 5, element 8) which generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (column 6, line 35-42 and 56-65; column 9, line 59-68).

Regarding claims 4 and 11, Tanaka discloses that a sequencer determines which direction each function operates in for a given matrix (figure 6, element 18; column 11, line 16-17).

Regarding claims 5 and 12, Tanaka discloses that an address generator which generates an address for each coefficient in the matrix (column 5, line 55-59).

Regarding claims 6 and 13, Tanaka discloses that the functions concurrently executed in the same direction on two different matrices of coefficients (column 11, line 16-40; column 12, line 4-10).

Regarding claims 7 and 14, Tanaka discloses that the functions are concurrently executed in the same direction (column 12, line 4-10), the functions switching periodically and concurrently to the other direction (column 11, line 16-40; column 15, line 10-28).

Regarding claim 28, Tanaka discloses that said second one-dimensional inverse discrete cosine transforming function and said third one-dimensional inverse discrete cosine transforming function occur concurrently in the same direction (column 11, line 16-40; column 15, line 10-28).

(10) Response to Argument

(A) The following discussion relates to the rejection of claims 1, 4-8, 11-15, 19-21, 23-25 and 28 under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (USPN 5,268,853, hereafter Tanaka).

1. Appellant's Argument – Appellant argues on page 8, first paragraph with respect to claims 1 and 5 (claims 8 and 12 are similarly rejected), "The rejection contends that Tanaka describes an arrangement in which both of the inverse discrete coefficient (DCT) calculators operate in the same direction (i.e., column or row) at the same time. Tanaka, and specifically col. 11, lines 9-40 of Tanaka, does not disclose or suggest such an arrangement."

Examiner's Response – The examiner respectfully disagrees. The examiner would first like to discuss the claim language. Claim 1 outlines a method of implementing a two-dimensional inverse discrete cosine transform (DCT) comprising executing first and second one-dimensional inverse DCT functions in first and second separate inverse DCT calculators, each of the first and second functions being controlled to operate on a matrix of coefficients with **both** of said first and second inverse DCT calculators operating **simultaneously** in a row direction at a first time, and with **both** of said first and second inverse DCT calculators operating **simultaneously** in a column direction at a second time (emphasis added). The examiner would first like to point out that Tanaka describes the construction of discrete cosine transform (DCT) and *inverse* DCT as being interchangeable (Tanaka, column 4, line 61-68; column 13, line 23-25).

The examiner would next like to point out that claim 1 does not contain any limitation that the first and second separate inverse DCT calculators read to or write from the same memory device, nor is there any mention of a memory device. In addition, the transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., Invitrogen Corp. v. Biocrest Mfg., L.P., 327 F.3d 1364, 1368, 66 USPQ2d 1631, 1634 (Fed. Cir. 2003) ("The transition comprising in a method claim indicates that the claim is open-ended and allows for additional steps."); Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.); Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 229 USPQ 805 (Fed. Cir. 1986); In re Baxter, 656 F.2d 679, 686, 210 USPQ 795, 803 (CCPA 1981); Ex parte Davis, 80 USPQ 448, 450 (Bd. App. 1948) ("comprising" leaves "the claim open for the inclusion of unspecified ingredients even in major amounts"). See MPEP § 2111.03.

Merriam-Webster's Collegiate Dictionary (Tenth Edition) defines the word "simultaneous" as existing or occurring at the same time: exactly coincident. The following description in Tanaka explicitly describes the operation of two one-dimensional DCT calculators 4 and 6 that operate in the same direction at the same time.

Tanaka discloses that in an initial phase, a first one-dimensional discrete cosine transformation (DCT) calculator 4 calculates the DCT of a first matrix of data, the results

of which are written to a memory device 2 in a row direction (memory location addresses are designated in a row direction, e.g. (0,0), (1,0), (2,0), etc.; Figure 5; column 11, line 9-15). Simultaneously, a second one-dimensional DCT calculator 6 is reading the data from the memory in a row direction that was previously written to the memory device in a column direction in the previous phase, but since this is the initial phase, the data stored therein (before being written to by the first DCT calculator) is meaningless.

In the next phase, the address direction is switched to designate addresses in a column direction (e.g. (0,0), (0,1), (0,2), etc.; column 11, line 16-20). The first DCT calculator 4 inputs a new matrix of data and begins calculating the DCT in a column direction. The first memory location (0,0) of the memory device containing the data previously written by the first DCT calculator 4 is read and transmitted to the second one-dimensional DCT calculator 6 (which performs a second DCT calculation in a column direction), and the calculated results of the DCT calculated by the first one-dimensional DCT calculator 4 are written to the same address (0,0) in the column direction (column 11, line 20-24). Then the memory address is changed to (0,1) (incremented in the column direction) and the second one-dimensional DCT calculator 6 reads data of this address (column 11, line 24-26). Subsequently, the calculated results of the first one-dimensional DCT calculator 4 are written to this address (0,1) as data and such reading and writing operations are repeatedly performed in a column direction until the last memory address (column 11, line 26-34). For further illustration, Figure 9

shows a timing diagram detailing the read and write operations occurring at each time step (Tanaka, column 10, line 64-column 11, line 5).

This description explicitly shows that both one-dimensional DCT calculators operate simultaneously in the same direction. During a read/write cycle, at a first time step (clock), the second DCT calculator 6 reads data from a memory location that was written by the first DCT calculator 4 in a previous phase in a different direction. Subsequently, the first DCT calculator 4 writes newly calculated data to the memory location, which data will be read by the second DCT calculator during the following phase in a different direction. At a second time step, the memory address is incremented and the second DCT calculator 6 again reads the data, after which the first DCT calculator 4 writes newly calculated data to the memory location. This alternate reading and writing continues with both DCT calculators operating in the same direction until the last memory location. The examiner would like to point out that even though the two DCT calculators do not simultaneously read and write the same memory location; that does not mean that the DCT calculators are not operating simultaneously in the same direction.

Tanaka then discloses that the row and column addresses in the memory device are again switched at which time the second one-dimensional DCT calculator 6 reads data out of each memory address in a row direction and the calculated results of the first one-dimensional DCT calculator 4 are alternately written to the same address until the last address (column 11, line 34-40; see also column 10, line 26-31 and 59-63). This explicitly shows that the one-dimensional DCT calculators 4 and 6 operate

simultaneously in the same direction, alternately reading and writing each memory location in one direction until the entire memory has been read by the second DCT calculator 6 and written by the first DCT calculator 4, at which time the direction is again switched so that the DCT calculation may be performed in the other direction orthogonal to the first. This ensures that both one-dimensional DCT calculations occur in each of the column and row directions for a given matrix of data.

2. Appellant's Argument – Appellant argues on page 9, last paragraph, "Tanaka's first one-dimensional DCT calculator executes a DCT formula in a row direction and the second one-dimensional DCT calculator executes a formula in the column direction (see, inter alia, Tanaka col. 7, lines 56-63, col. 8, lines 29-37). Tanaka also states that a switching circuit may cause the addresses in the memory device to switch to a row direction during a reading operation and thereafter switch to a column direction for a writing operation (see, inter alia, Tanaka col. 10, lines 20-24)."

Examiner's Response – The first two sections cited by appellant, column 7, line 56-63 and column 8, line 29-37, disclose the conventional operation of a two-dimensional discrete cosine transformation which inherently must be performed in two directions, either column direction first and then row direction, or row direction first and then column direction. This is why Tanaka has provided a switching circuit 18 to switch the operating directions of both one-dimensional DCT calculators 4 and 6 such that the second one-dimensional DCT calculator 6 reads the calculated results of the first one-dimensional DCT calculator 4 from the memory 2 in a direction different from that in which the results were originally written to the memory, while, simultaneously, the first

one-dimensional DCT calculator 4 writes newly calculated results in the same direction as the reading direction of the second one-dimensional DCT calculator 6.

As to applicant's second argument, with respect to column 10, line 20-24 in Tanaka, the appellant is referring to a different embodiment of the cited reference than the examiner is relying on for support of the anticipation of appellant's invention. Column 9, line 46 in Tanaka states that the following description encompasses the first embodiment of the invention, while column 10, line 64 states that the following description relates to another embodiment, which goes on to describe the operation cited by the examiner in column 11.

3. Appellant's Argument – Appellant argues on page 10 first and second paragraphs, "The rejection alleges, that Tanaka describes calculators operating simultaneously in the same direction (see, inter alia, Advisory Action of October 14, 2004, continuation of 5). However, there is no support for this position. It is respectfully submitted that Tanaka simply fails to disclose calculators simultaneously operating in the same direction. Accordingly, as Tanaka fails to disclose the one-dimensional DCT calculators operating in the same direction at the same time, claims 1 and 5 should be allowable."

Examiner's Response – The examiner respectfully disagrees. The examiner feels that a prima facie showing of anticipation has been satisfied, (see above discussion in section (A) 1). Appellant has not shown the examiner exactly why there is no support for the rejection. A mere statement of lack of support is insufficient to overcome the rejection.

4. Appellant's Argument – Appellant argues on page 10, third paragraph with respect to claim 4 (rejected together with claim 11), "Claim 4 is independently allowable as Tanaka does not consider using a sequencer for determining the direction of operation for a function for a given matrix. Rather, Tanaka uses a switching circuit to switch, for example, a writing operation to occur in a column direction and a reading operation to occur in a row direction (see, inter alia, Tanaka col. 10, lines 27-31)."

Examiner's Response – The examiner respectfully disagrees. Claims 4 and 11 were rejected on the basis that the switching circuit 18 functions as a sequencer that determines which direction each DCT function operates in for a given matrix (Figure 6; column 11, line 16-17). Merriam-Webster's Collegiate Dictionary (Tenth Edition) defines "sequencer" as one that sequences such as a device for arranging in a sequence. In this case, the switching circuit 18 serves to sequence the direction in which each DCT function operates for a given matrix by alternating the sequence between the row and column directions. The examiner would also like to point out that the switching circuit 18 is considered to be part of the address generator 8, which designates an address of the memory device 2 and replaces row and column addresses with each other in accordance with a switching operation of writing and reading operations of the memory device 2 (column 6, line 35-42).

5. Appellant's Argument – Appellant argues on page 10, fourth paragraph with respect to claim 6 (rejected together with claim 13), "Claim 6 is also independently allowable as Tanaka does not describe the concurrent execution of the functions in the same direction on two different matrices of coefficients. Tanaka describes concurrent

execution in two directions and describes operations relating to a single matrix of coefficients (e.g., the reading and writing operations pertaining to the memory device)."

Examiner's Response – The examiner respectfully disagrees. The examiner again asserts that the two one-dimensional DCT calculators 4 and 6 do not operate in different directions at the same time. The operation described at column 11, lines 9-40 explicitly shows that a first matrix of discrete cosine transformation results calculated by the first DCT calculator 4 are first written to the memory device 2 in a first (row) direction. Next, the switching circuit 18 of the address generator is operated to switch the row and column addresses so that the second DCT calculator begins reading the memory in a second (column) direction different in than the first (row) direction. After the second DCT calculator reads the first memory location containing data from the first matrix written to the memory by the first DCT calculator, the first DCT calculator writes the results of a newly calculated discrete cosine transformation of a second matrix into the same memory location. At each memory location, the second DCT calculator first reads the data of the first matrix from the first calculation by the first DCT calculator, and then the first DCT calculator writes new data of a second matrix of a second calculation to the same memory location until the last memory location, when the address direction is again switched.

6. Appellant's Argument – Appellant argues on page 10, last paragraph onto page 11 with respect to claim 7 (rejected together with claim 14), "Claim 7 is also independently allowable as Tanaka fails to disclose both the concurrent execution of the

two functions in the same direction, as well as the periodic and concurrent switching between the row and column directions."

Examiner's Response – The examiner respectfully disagrees. The examiner believes that it has been shown that the two one-dimensional DCT calculators 4 and 6 do indeed operate concurrently in the same direction and that the switching circuit 18 ensures the periodic and concurrent switching between the row an column directions (see above discussion in sections (A) 1-3).

7. Appellant's Argument – Appellant argues on page 11, sixth and seventh paragraphs, "Claim 15 and claim 28 dependent thereon, require the first and second inverse discrete cosine calculators to concurrently execute transforming functions in the column direction. These claims are also allowable because Tanaka, as noted above, does not disclose the concurrent execution of transforming functions in the same direction. Furthermore, claim 15 covers the concurrent and periodic switching of directions, a feature that is not disclosed in Tanaka. Similar to claim 15, claim 19 also provides for concurrent and periodic switching of transforming functions, and as a result, this claims should also be allowable."

Examiner's Response – The examiner respectfully disagrees. As discussed above with respect to claims 7 and 14, the examiner believes that it has been shown that the two one-dimensional DCT calculators 4 and 6 do indeed operate concurrently in the same direction and that the switching circuit 18 ensures the periodic and concurrent switching between the row an column directions (see above discussion in sections (A) 1-3).

8. Appellant's Argument – Appellant argues on page 11, last paragraph onto page 12, "Claim 23 includes a sequencer block that is alternately in a first state to control a column direction of operation of both one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation of both one-dimensional inverse discrete cosine transform blocks. As both of the first and second states provide that the transform blocks are operating in the same direction (in both of the two operating states), these claims are not anticipated by Tanaka. In addition, Tanaka does not describe controlling the two transform blocks to cause them to operate in a single direction."

Examiner's Response – The examiner respectfully disagrees. The examiner believes that it has been shown that the switching circuit 18 operates as a sequencer block that is alternately in a first state to control a column direction operation of both one-dimensional DCT blocks 4 and 6, and in a second state to control a row direction of operation of both one-dimensional DCT blocks 4 and 6 (see above discussion in sections (A) 1-4).

9. Appellant's Argument – Appellant argues on page 12, second paragraph, "Claim 25 defines a sequencer block that alternates between a first state which controls both of the first and second one-dimensional inverse discrete cosine transform blocks to operate in a row direction, and a second state which controls both of said first and second one-dimensional inverse discrete cosine transform blocks to operate in a column direction. The sequencer block is alternately in one of two states, each state indicating the direction of operation of both one-dimensional inverse discrete cosine

transform block. Tanaka does not disclose controllable states in which both transform blocks are operating in the same direction, and as such, claim 25 should be allowable."

Examiner's Response – The examiner respectfully disagrees. The examiner believes that it has been shown that the switching circuit 18 operates as a sequencer block that alternates between a first state to control both one-dimensional DCT blocks 4 and 6 to operate in a row direction, and in a second state to control both one-dimensional DCT blocks 4 and 6 to operate in a column direction (see above discussion in sections (A) 1-4).

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Craig Kronenthal
February 13, 2006

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